A True Two-Quadrant Fully Integrated Switched Capacitor DC-DC Converter Supporting Vertically Stacked DVS-Loads With Up To 99.6% Efficiency

Athanasios Sarafianos, Michiel Steyaert
Department of Electrical Engineering, ESAT-MICAS - KU Leuven, Leuven, Belgium
asarafia@esat.kuleuven.be, steyaert@esat.kuleuven.be

Abstract

This paper presents a Switched Capacitor DC-DC converter capable of powering two vertically stacked loads, unlocking efficiencies of up to 99.6% when loads consume identical current. Furthermore, this converter is the first to provide up to 100% current imbalance thanks to its true two-quadrant operation, allowing loads to completely turn off. The system has been fabricated in a 65nm GP process followed by validation through measurements of its high efficiencies (>90% when δI<0.4) and control loop operation.

Introduction

While many Switched-Capacitor (SC) DC-DC converters show great potential for full integration alongside the load, most provide power to only a single load [1]. Few, however, have ventured into the domain of stacking loads in series, or vertically, enabling efficiencies close to 100% [2–5]. When vertically stacked loads consume identical current, the load voltages are implicitly converted, similar to a resistive divider, leaving the DC-DC converter essentially idle. When the load currents exhibit an imbalance, a DC-DC converter needs to provide this imbalance to the intermediate node by either sourcing or sinking current to attain the desired load voltages.

While non-SC DC-DC converters exist that can deliver bidirectional power [4-5], recent SC converters fail to grasp the implications of two-quadrant operation [2-3]. For example, a 2:1 SC converter supplying two stacked loads Vin can never achieve equal load voltages, since any current flowing through the converter due to current mismatch imposes a voltage drop over its output impedance (Fig. 1), leading to unequal load voltages [3]. This is solved by providing two Voltage Conversion Ratios (VCR), one to compensate forward voltage drops over Rout (sourcing current), the other to compensate reverse voltage drops (sinking current) [6]. In this work, a SC DC-DC converter is presented that implements two VCRs for sourcing and sinking when Vload1 = Vload2, and an additional VCR for increasing overall efficiency when Vload1 ≠ Vload2 (Fig. 6). This allows the converter to provide load voltages of 0.75-1.1V, enabling Dynamic Voltage Scaling [1]. A fully integrated control loop regulates the output voltage and selects the ideal VCR. To the authors' best knowledge, this is the first monolithic two-quadrant SC converter, with a fully integrated control loop, capable of dealing with up to 100% load imbalance, and achieving efficiencies up to 99%.

System Overview

Fig. 1 shows an overview of the implemented converter, consisting of three blocks. The power converter is partitioned into eight fragments that contain an in-phase and an opposite-phase power train, to homogenize the output ripple. A hysteretic controller ensures stable operation of the converter, using either the positive (sourcing) or the negative (sinking) output of the clocked comparator. The selected toggling signal is then fed to a ring of SR-latches that generate the switching frequency for each fragment. Finally, two modified clocked comparators with hysteresis are used to select the correct VCR.

Fig. 2 shows how topology selection is performed. This converter uses three VCRS, namely 3:2 (T_{23}=1), 3:1 (T_{13}=1) and 2:1 (T_{13}=0 and T_{23}=0). While ratio 3:2 is exclusively used for sourcing and ratio 3:1 exclusively for sinking, ratio 2:1 can be used for either, depending on ratio N=Vload1 Vload2 . As long as N>1, ratio 2:1 will be used for sinking, whereas ratio 2:1 is used for sourcing when N<1. However, when N=1, ratio 2:1 cannot be used, since the voltage drop over the output impedance prohibits these operating points. Hence, a band of hysteresis, set by V_{lvl}, is applied along N=1, using VCR 3:2 for sourcing or 3:1 for sinking. The second comparator monitors the intermediate node, and decides whether the converter needs to source (SRC) or sink (SNK) current. As long as the output voltage remains within a boundary set by V_{bhyst}, no changes in topology occur. However, when the output voltage crosses this boundary, the comparator will change modes (SRC↔SNK), after which the output voltage recovers. Combining the comparator outputs yields the desired VCR.

Fig. 3 shows the transistor implementation of the power converter and the capacitor arrangement of each VCR in their 2-phase operation. While most transistors are thin-oxide devices, M_9 has been implemented as two thick-oxide devices, being subject to widely varying terminal voltages. Capacitors $C_{1\text{-}2}$ are each 37.7pF, implemented as a stacked MIM-MOM structure. Due to the symmetrical nature of this combination of VCRs, two transistors, namely M_6 and M_3, undergo a drain-source reversal, which might lead to unwanted turn-on of the device. For example, in mode T_{23}, the drain of transistor M_6 is connected to V_{in} in φ_1 ($V_{drain}>V_{source}$), yet drops below V_{out} in φ_2 ($V_{drain}<V_{source}$). To prevent M_6 turning on in φ_2, the pass-gate multiplexer connects the gate of M_6 to capacitor node $C_{1\text{-}}$, which prevents the transistor turning on in either phase. When operating in another VCR, the multiplexer selects the gate drive from the buffer chain.

Measurement Results & Conclusion

A test chip is realized in a 65nm CMOS process. The measurement results in Fig. 4 characterize the converter efficiency in two cases. The first shows the greatest potential: for the given set of operating points, assuming one load is always fully on, efficiencies reach more than 90% for δI<0.4, and reach >98% when load currents are nearly identical. The second measurements show the efficiencies of the converter when one of the loads is completely idle (I=0mA). Even in this case, a peak efficiency of 80% is achieved, while at the quoted power density in Fig. 7 an efficiency of 73% is recorded. Fig. 6 highlights up to 16% efficiency improvement by implementing VCR 2:1 for no additional area cost.

The transient response measurements in Fig. 5 are performed using an on-chip programmable load. All load transients occur at a rise time of 100ps, from simulation. In all measured transients, overshoot/undershoot is limited by the hysteresis of the control loop of Fig. 2. Once crossed, the comparator switches from SRC↔SNK, and the output voltage recovers. A maximum droop of 75mV is observed when switching from sinking to sourcing. The converter is stable at zero-load, settling back to sourcing in this case.

Fig. 7 compares this work to other recent SC converters [1-2] and two-quadrant power converters [3-4]. In [2], bidirectional current is severely limited (<16%), while only coarse regulation is provided. The SC converter of [3] claims two-quadrant operation, yet has no control loop, and suffers steady-state droop. The push-pull linear regulator in [4] provides true two-quadrant operation, yet efficiency is limited by the power consumption of its linear regulators. The work presented in this paper supports up to 100% current imbalance, boasts a fully integrated control loop for true two-quadrant operation, and achieves very high efficiencies of up to 99.6%.

References

[1] Yan Lu, et al., ISSCC, pp.1-3, Feb. 2015
[2] Lee, S. K., et al., VLSI, pp.318-319, June 2015
[3] Chang L., et al., VLSI, pp.55-56, June 2010
[4] Rajapandian S., et al., JSSC, pp.1400-1410, June 2006
[5] Schaef C., et al., TPEL, pp.1795-1808, Feb. 2016
[6] Sarafianos A., et al., COMPEL, pp.1-6, June 2016

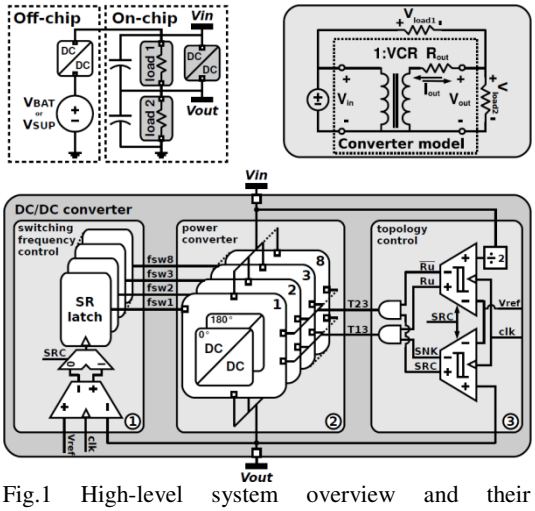

Fig.1 High-level system overview and their implementation (control loops and power converter).

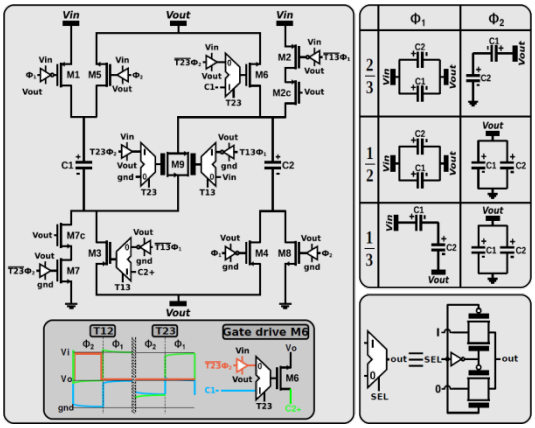

Fig.3 Transistor-level implementation of one fragment of the power converter, consisting out of 9 switches and 2 capacitors, capable of operating in VCRs 3:2, 2:1 and 3:1. Sample operation of M6 is shown below.

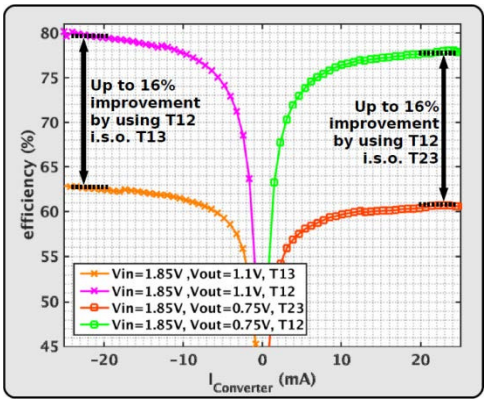

Fig.6 While VCRs 3:2 and 3:1 cover the desired ranges of the loads, the addition of VCR 2:1 at no additional cost allows an efficiency improvement of up to 16% for the quoted operating ranges.

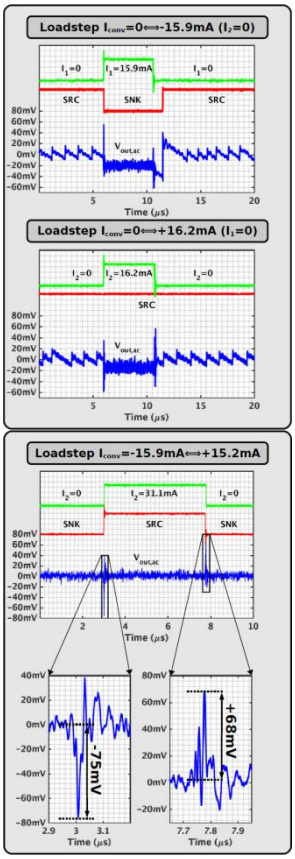

Fig.5 Transient measurements.

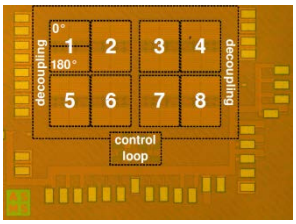

Fig.8 Chip micrograph for a total active area of 0.796mm^2.

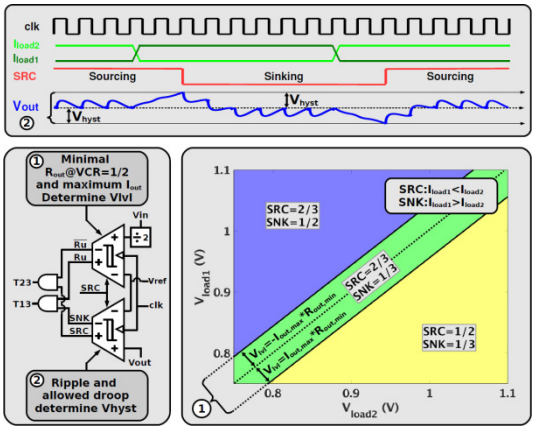

Fig.2 Topology selection is done by combining the output of two clocked comparators: one that monitors the output node (SRC/SNK), the other comparing both voltage domains (Ru).

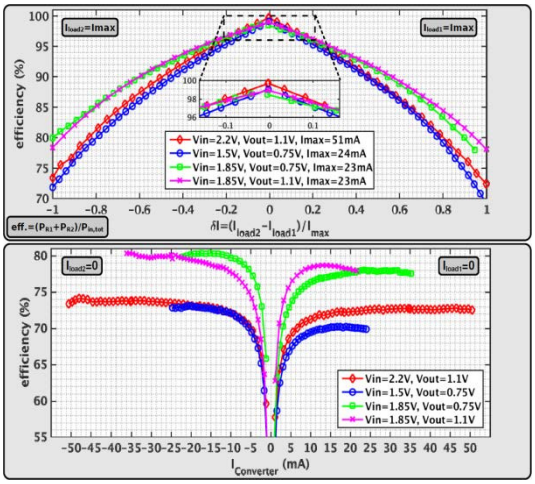

Fig.4 Measured system efficiency when one load consumes maximum current, and converter efficiency (one of two loads turned off). When loads are closely matched, only the stand-by power of the converter limits efficiency (>98%).

Reference	This Work	ISSCC15 [1]	VLSI15 [2]	VLSI10 [3]	JSSC06 [4]
Tech.	65nm GP	65nm	40nm G	45nm SOI	180nm
V_{in}[V]	1.5-2.2	1.6-2.2	3.6	2	5.4
V_{out}[V]	0.75-1.1	0.6-1.2	2.7;1.8;0.9	1	3.6;1.8
$I_{out,max}$[mA]	±51	+175	±1.56	±2.5	±65
$(\delta I)_{max}$	100%	N.A.†	15.7%	60%	66%
control loop	yes	yes†	yes††	no	yes
V_{droop}[mV]	75@100ps	58@100ps	87.5	150/50	N.A.
VCRs	3:1,2:1,3:2	2:1,3:2,4:3	4-lvl sym. ladder	2:1	0.5
type conv.	SC	SC	SC	SC	lin. reg.
η_{conv}@ρ*	73	78.3	68	90	46.9
η_{system}	98-99.6	78.3	97-99.8	96-99	80
ρ_{conv}	70*/140**	180	N.A.	2300*/4600**	N.A.

†single load SCPC ††coarse C-modulation *for single load** for stacked loads

Fig.7 Comparison with the state-of-the-art. [1] Single load SC converter with similar performance. [2] Stacked loads converter with limited closed-loop sourcing and sinking capabilities. [3] open-loop SC (trenchcap) converter. [4] push-pull linear regulator.